AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A ~~digital integrated circuit~~ BTSC signal encoder ~~for encoding audio signals~~, comprising:

~~(A)~~ a first low pass filter to receive and filter a digital left channel audio signal and a right channel audio signal, in which the first low pass filter operates as a higher order ~~IIR~~ infinite impulse response (IIR) digital filter implemented using an allpass decomposition architecture;

~~(B)~~ matrix means ~~for receiving a digital~~ coupled to receive filtered left channel audio signal and ~~a digital~~ right channel audio signal, ~~comprising means for summing said digital~~ sum the filtered left and right channel audio signals ~~and thereby generating~~ to generate a digital sum signal, and ~~including means for subtracting~~ subtract one of ~~said digital~~ the left ~~and~~ or right channel audio ~~signals~~ signal from the other of ~~said digital~~ the left ~~and~~ or right channel audio ~~signals and thereby generating~~ signal to generate a digital difference signal;

~~(C)~~ sum channel processing means ~~for processing said~~ coupled to process the digital sum signal; ~~and~~

~~(D)~~ difference channel processing means ~~for digitally processing said~~ coupled to process the digital difference signal, wherein the difference channel processing means includes a wideband amplifier and a spectral compressor, in which a gain for the wideband amplifier is set by a wideband gain feedback loop and a gain for the spectral compressor is set by a spectral gain feedback loop; and

a second low pass filter to receive and filter an output of the difference channel processing means, in which the second low pass filter operates as a higher order IIR digital filter implemented using an allpass decomposition architecture and in which an output from the second low pass filter is coupled for processing with an output of the sum channel processing means and also coupled as feedback input to the wideband gain feedback loop and to the spectral gain feedback loop;

wherein the ~~higher order IIR digital~~ first and second low pass filters, matrix means, sum channel processing means and the difference channel processing means operate at a ~~first~~ sample rate to substantially match BTSC analog filter transform functions in both magnitude and phase.

2. (currently amended) The BTSC signal encoder of claim 1, wherein the ~~higher order IIR digital filter comprises a~~ first and second low pass filters are Cauer low pass filters.

3. (currently amended) The BTSC signal encoder of claim 1, ~~wherein the higher order IIR digital filter comprises an input low pass filter~~ further including a third low pass filter coupled to receive and filter an output of the sum channel processing means, in which the third low pass filter operates as a higher order IIR digital filter implemented using an allpass decomposition architecture.

4. (canceled)

5. (currently amended) The BTSC signal encoder of claim 1, wherein ~~the higher order IIR digital filter comprises~~ each of the low pass filters includes a sum of multiple cascades of lower order allpass filters.

6. (currently amended) The BTSC signal encoder of claim 5, wherein each of the cascade of lower order allpass filters ~~comprises a~~ implements a combination of first ~~or~~ and second order allpass filters.

7. (currently amended) The BTSC signal encoder of claim 1, wherein the ~~higher order IIR digital filter comprises a~~ first and second low pass filters are Butterworth low pass filters.

8. (currently amended) The BTSC signal encoder of claim 1, wherein the ~~higher order IIR digital filter comprises a pre-emphasis filter in the BTSC encoder~~ matrix means

includes at least one preemphasis filter which is a higher order IIR digital filter implemented using an allpass decomposition architecture.

9. (currently amended) The BTSC signal encoder of claim 1, wherein ~~the higher order IIR digital filter comprises a bandpass filter in the BTSC encoder~~ the difference channel processing means includes a bandpass filter which is a higher order IIR digital filter implemented using an allpass decomposition architecture.

10-11. (canceled)

12. (currently amended) The ~~integrated circuit digital BTSC encoder of claim 11, wherein the higher order digital filter comprises a Cauer low pass filter~~ BTSC signal encoder of claim 1, wherein the BTSC signal encoder operates at the sample rate of approximately 150-200 KHz.

13. (canceled)

14. (currently amended) The ~~integrated circuit digital~~ BTSC signal encoder of claim ~~11~~ 1, wherein the ~~higher order digital filter comprises an eleventh order Cauer low pass IIR filter~~ first and second low pass filters are eleventh order Cauer low pass filters.

15. (currently amended) The ~~integrated circuit digital~~ BTSC signal encoder of claim 14, wherein ~~the cascade of lower order allpass filters comprises a first order allpass filter and a plurality of second order allpass filters~~ each of the eleventh order Cauer low pass filters implements a combination of first and second order allpass filters.

16. (currently amended) The ~~integrated circuit digital~~ BTSC signal encoder of claim ~~11~~ 14, wherein ~~the higher order digital filter comprises a Butterworth low pass filter~~ each of the eleventh order Cauer low pass filters implements a combination of one first order and five second order allpass filters.

17. (currently amended) The ~~integrated circuit digital~~ BTSC signal encoder of claim ~~11~~ 1, wherein the ~~sum channel processor, difference channel processor and higher order digital filter are~~ BTSC signal encoder is fabricated on a single silicon substrate using CMOS processing.

18-19. (canceled)

20. (currently amended) ~~A single chip~~ The BTSC signal encoder of claim 1 in which the BTSC signal encoder is implemented in a set top box ~~integrated circuit digital BTSC encoder that is operable to encode first and second digital audio signals into a BTSC encoded signal, comprising a higher order IIR filter implemented using an allpass decomposition filter structure comprising a sum of two allpass filter stages, where each allpass filter stage comprises a plurality of lower order allpass IIR filters~~.

21. (canceled)